TCET/FRM/IP-02/10 Revision: B

**Semester Plan**
**(Practical / Tutorials / Assignment)**

Semester: **III** Course: **IT** Batches: **S.E (B4)**

Subject: **Digital design Lab** Class: **SE – IT** Batch size: **20** Students

Laboratory faculty in charge: **Mr.Yele V.P.**
Lab. Assistant /Attendant: **Mr.Vaibhav Chavan (Lab Attendant )**

Note: **Experiment planned as per University Curriculum**

| **Basic Experiments:** | | | | |
|---|---|---|---|---|
| **Sr. No.** | **TITLES Experiments / Tutorials / Assignment (Planning with use of Technology)** | **Planned Date** | **Completion Date** | **Remarks** |
| **1** | Verify the truth table of logic gates (basic and universal gates) | 24/7/17 | | |
| **2** | Realization of Boolean algebra using gates | 31/7/17 | | |
| **3** | Verify the operation of 4- bit magnitude comparator | 7/8/17 | | |
| **4** | Implementation of Multiplexer and De-Multiplexer using Gates | 14/8/17 | | |
| **5** | Implementation of Encoder and Decoder using Gates | 14/8/17 | | |
| **Design/ Development Experiments:** | | | | |
| **6** | Design of Full Adder and Full Subtractor | 4/9/17 | | |
| **7** | To verify and observe the operation of SR and JK flip-flops | 11/9/17 | | |

| Issued By: MR | Approved By: Principal |
|---|---|

| | | | | |
|---|---|---|---|---|
| **8** | To design and verify Left and Right shift registers | 11/9/17 | | |
| **9** | Implementation of Logic Gates using VHDL | 18/9/17 | | |
| **Group Learning Activity:** | | | | |
| **10** | **Case Study on:**<br>Case study on Evaluating and observing Boolean expression using PALs and PLAs | 18/9/17 | | |
| **11** | **Project:**<br>1. To design automated system for washing machine<br>2. To design control system for lift | **25/9/17** | | |

**Mini /Minor Projects Objective:** To get hands on experience to execute projects with respect to student choice in the following areas. **(30 Hrs / Semester / Student). (Total 120 Hrs)**

**The areas are:**

**1. Research 2. Core 3. Multidisciplinary 4. Application**

| **S.No** | **Project Title/Group Size** | **Class** | **Group Size/ Project Hours** | **Project Type** | **Reference** |
|---|---|---|---|---|---|
| 1 | Simple Logic Gate Processor | SE | 4-5 | Mini | http://circuiteasy.com/logic-gates/ |
| 2 | Learn to Make NAND Gate | SE | 4-5 | Mini | http://circuiteasy.com/nand-gate |
| 3 | Literature survey on IoT for Agriculture | SE | 4-5 | Mini | www. e lsevier.com/ locate/csi |
| 4 | Literature survey IoT for<br>Envirnoment management | SE | 4-5 | Mini | www. e lsevier.com/ locate/csi |
| | | | | | |

| No. | Planned | Completed | No. of | Planned | Completed | No. of | Planned | Completed |
|---|---|---|---|---|---|---|---|---|

| | |
|---|---|
| Issued By: MR | Approved By: Principal |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| of Prac | **Basic Exp:** 03 **Design Base Exp**: 06 **Group Learning:** 02 **Mini Project:** 2 **Case study:** 1 | | Assign ments | 03 | | Tutorial | ----- | ------ |

| | |
|---|---|
| DOSLNE: | DOSLE (engaged in some other dates): |

Group activities are required to be added with the practical related to course to enhance the learning activity of the student in the course. Group activity includes: Group presentation, new experiment design, mini projects etc.

**Note:**

1. The practical plan date and completion date shall be in compliance. For any non-compliance reason(s) required to be stated in remark column.
2. Learning objective and outcome shall be clearly stated with each of experiments/ tutorials/ assignments and are required to be mapped at the end of the semester.
3. Entry for DOSLE (engaged on some other date) shall be done with proper mapping to DOSLNE.

**(Ms. Swati Abhang)**
**(Mr. Yele Vijaykumar)**

| Name & Signature of Faculty | Signature of HOD | Signature of Principal / Dean Academic |
|---|---|---|
| Date: 12/07/2017 | Date: | Date: |

| | |
|---|---|
| Issued By: MR | Approved By: Principal |