**Department of E&TC**
**Microprocessors and Peripherals (Rev to CBGS) Mock Paper for September 2020**

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| 1 | 8085 microprocessor is called 8-bit microprocessor because<br>a. The address bus is of 8-bits<br>b. The data bus is of 8 bits<br>c. It has 8 control signals<br>d. It operates in 8 modes | (1) |
| 2 | The control of data bus buffer in 8255 is done by<br>a. control word register<br>b. read/write control logic<br>c. data bus<br>d. ALE | (1) |
| 3 | The port that is used for the generation of handshake lines in mode 1 or mode 2 is<br>a. port A<br>b. port B<br>c. port C Lower<br>d. port C Upper | (1) |
| 4 | In BSR mode of 8255, only port C can be used to<br>a. set individual ports<br>b. reset individual ports<br>c. set and reset individual ports<br>d. programmable I/O ports | (1) |
| 5 | Which of the following instruction is not valid?<br>a. MOV AX, BX<br>b. MOV DS, 5000H<br>c. MOV AX, 5000H<br>d. PUSH AX | (1) |
| 6 | The instructions that are used for reading an input port and writing an output port respectively are<br>a. MOV, XCHG<br>b. MOV, IN<br>c. IN, MOV<br>d. IN, OUT | (1) |
| 7 | The instruction that loads effective address formed by destination operand into the specified source register is<br>a. LEA<br>b. LDS<br>c. LES<br>d. LAHF | (1) |
| 8 | This instruction is used for adding the carry<br>a. ADDC<br>b. ADD<br>c. ADC<br>d. ADD & ADC | (1) |
| 9 | he instruction, {MOV AX, 16-bit data} belongs to the address mode<br>a) register<br>b) direct<br>c) immediate<br>d) register relative | (1) |
| 10 | The instruction that subtracts 1 from the contents of the specified register/memory location is<br>a) INC<br>b) SUBB<br>c) SUB<br>d) DEC | (1) |
| 11 | The instruction, CMP to compare source and destination operands it performs<br>a) addition<br>b) subtraction<br>c) division<br>d) multiplication | (1) |

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| 12 | In the RCL instruction, the contents of the destination operand undergo function as<br>a) carry flag is pushed into LSB & MSB is pushed into the carry flag<br>b) carry flag is pushed into MSB & LSB is pushed into the carry flag<br>c) auxiliary flag is pushed into LSB & MSB is pushed into the carry flag<br>d) parity flag is pushed into MSB & LSB is pushed into the carry flag | (1) |
| 13 | The instructions that are used to call a subroutine from the main program and return to the main program after execution of called function are<br>a) CALL, IRET<br>b) JMP, IRET<br>c) CALL, RET<br>d) JMP, RET | (1) |
| 14 | Which assembler directive is used to direct the assembler to reserve words<br>a. DB<br>b. DD<br>c. DW<br>d. DT | (1) |
| 15 | The number of instructions actually executed by the microprocessor depends on the<br>a) stack<br>b) loop count<br>c) program counter<br>d) time duration | (1) |
| 16 | Example of an external interrupt is<br>a) divide by zero interrupt<br>b) keyboard interrupt<br>c) overflow interrupt<br>d) type2 interrupt | (1) |
| 17 | The operation that can be performed on control word register is<br>a) read operation<br>b) write operation<br>c) Move operation<br>d) copy operation | (1) |
| 18 | In timer 8253 If BCD=0, then the operation is<br>a) decimal count<br>b) hexadecimal count<br>c) binary count<br>d) BCD count | (1) |
| 19 | The register that stores all the interrupt requests in it in order to serve them one by one on a priority basis is<br>a) Interrupt Request Register<br>b) In-Service Register<br>c) Priority resolver<br>d) Interrupt Mask Register | (1) |
| 20 | When non-specific EOI command is issued to 8259A it will automatically<br>a) set the ISR<br>b) reset the ISR<br>c) set the INTR<br>d) reset the INTR | (1) |
| 21 | In 8257 (DMA), each of the four channels has<br>a) a pair of two 8-bit registers<br>b) a pair of two 16-bit registers<br>c) one 16-bit register<br>d) one 8-bit register | (1) |
| 22 | After connecting 8257, The pin that requests the access of the system bus is<br>a) HLDA<br>b) HRQ<br>c) ADSTB<br>d) None of the mentioned | (1) |
| 23 | Identify the instruction set for: IN AX, 0028 H | (1) |

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| | a. Data Transfer Instruction<br>b. Bit Manipulation Instruction<br>c. Program Execution Transfer Instruction<br>d. String Instruction | |
| 24 | What does this instruction do? lea SI,ARR<br>a. load starting address of ARR in SI<br>b. Copy data from ARR to SI<br>c. Load effective address for SI to variable ARR<br>d. Load SI data in ARR | (1) |
| 25 | While performing INC instruction, which flag is not affected?<br>a. AF<br>b. OF<br>c. PF<br>d. CF | (1) |
| 26 | _____ instruction gives two's complement<br>a. NEG<br>b. CMP<br>c. CPL<br>d. SUB | (1) |
| 27 | Which of the following is a prefix instruction?<br>a. MOVSB<br>b. REP<br>c. RET<br>d. MOV | (1) |
| 28 | How many ICWs are available in single 8259?<br>a. 1<br>b. 2<br>c. 4<br>d. 8 | (1) |
| 29 | Which address lines from microprocessor are directly connected to 8255?<br>a) A1<br>b) A0, A1<br>c) A1, A2<br>d) A0 to A7 | (1) |
| 30 | If this line is a logical 0, the microprocessor can read and write to the 8255<br>a. WR<br>b. RD<br>c. CS<br>d. RESET | (1) |
| 31 | In the timer 8254, if In control word format, if RL1=1, RL0=1 then the operation performed is<br>a) read/load least significant byte only<br>b) read/load most significant byte only<br>c) read/load LSB first and then MSB<br>d) read/load MSB first and then LSB | (2) |
| 32 | If more than one channel of 8257 requests service simultaneously, the transfer will occur as<br>a) multi transfer<br>b) simultaneous transfer<br>c) burst transfer<br>d) none of the mentioned | (2) |
| 33 | In 8086 is the queue is to be emptied, what should be the status of QS1, QS0 bits<br>a. QS1 = 0, QS0 = 0<br>b. QS1 = 0, QS0 = 1<br>c. QS1 = 1, QS0 = 0<br>d. QS1 = 1, QS0 = 1 | (2) |
| 34 | If 19 address lines are selected for memory interfacing, how much memory is interfaced?<br>a. 128kb<br>b. 1Mb | (2) |

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| | c. 256kb<br>d. 512kb | |
| 35 | 8254 is operating in counter 0 which loads LSB firs and then MSB using Mode 3 with BCD count. What data is to be loaded in CWR?<br>a. 36H<br>b. 37H<br>c. 44H<br>d. 73H | (2) |
| 36 | How many address lines are required to interface a EPROM of 4kb<br>a. 10<br>b. 11<br>c. 12<br>d. 13 | (2) |
| 37 | If the value of flag register is 00C0h, which of the flags are set?<br>a. Sign flag and zero flag<br>b. Trap flag and sign flag<br>c. Interrupt flag and zero flag<br>d. Carry flag and sign flag | (2) |
| 38 | For the following code, which flags are affected<br>MOV AL, ABh<br>MOV BL, 12h<br>ADD AL,BL<br><br>a. DF<br>b. ZF<br>c. PF<br>d. SF | (2) |
| 39 | 1. For type 8 vector, what is the starting address of the address<br>a. 0020h<br>b. 0032h<br>c. 0012h<br>d. 0016h | (2) |
| 40 | If the Code segment and IP register holds the data 1024h and 1A33h respectively. What is the effective address?<br>a. 11C73h<br>b. 1B354h<br>c. 2A57h<br>d. 2A570h | (2) |